REMARKS/ARGUMENTS

Claims 1-34 stand rejected in the outstanding Official Action. Claims 1, 7-10, 13, 18, 22-28, 30-32 and 34 have been amended and therefore claims 1-34 remain in this application.

The Examiner's indication that the formal drawings previously filed are accepted is appreciated. Additionally, the Examiner's consideration of the prior art submitted with Applicants' Information Disclosure Statement is very much appreciated.

The Examiner objects to the abstract of the disclosure with respect to the reference to Figure 2, and this reference has been removed in the above amendment.

Claim 8 is objected to, with the Examiner suggesting that the word "wherein" be included. This amendment to claim 8 has been made, although the use of a linking term such as "wherein" is certainly optional and normally not required. However, the Examiner also cites Rule 75(i) as requiring "line indentation" in claim 8. Applicants point out that Rule 75(i) requires line indentation only when there is a "plurality of elements or steps" recited or added by that claim. Claim 8 adds only a single additional structure, i.e., the processor core, to the structure recited in claim 1. As a result, "line indentation" is not proper and indeed it is not certain where the line indentation would start, as only a single additional element is added in claim 8 to the structure previously recited in claim 1. Accordingly, any further objection to claim 8 under Rule 75(i) is respectfully traversed.

The Examiner correctly notes that claims 23 and 24 should have been dependent from claim 18, and they have been amended to properly depend from claim 18.

In view of the above amendments, there is believed no further basis for objection to any of the claims pending in Applicants' specification.

Claims 9-11, 13, 14 and 18-34 stand rejected under 35 USC §112 (second paragraph) as allegedly being indefinite. Claims 9 and 26 are rejected as allegedly being indefinite because the originally submitted claim language recites the limitation that the memory is "one of a synthesized memory and a custom memory." This language which the Examiner finds uncertain is well-recognized Markush claim form which has long been used in the U.S. Patent Office to avoid the use of alternative claiming, i.e., the use of the word "or" to indicate that the memory is chosen as one of several possible options, whether or not those options are equivalent. As a result, the Examiner's requirement for amendment of claims 9 and 26 is respectfully traversed. However, Applicants have amended the claim as suggested by the Examiner to use the word "or" and claim the two distinctly different memories in alternative form.

Claims 10 and 27 are argued as being indefinite because they use the term "adapted." The Examiner's attention is directed to the Manual of Patent Examining Procedure (MPEP) Section 2173.05(g) and the last paragraph thereof which specifically indicates that the Court of Customs and Patent Appeals in 1976 held that the phrase "adapted" serves to "precisely define present structural attributes of interrelated component parts of the claimed assembly" and is therefore not indefinite. Therefore, the Examiner's allegation that "adapted" is not a positive limitation is respectfully traversed. Notwithstanding the above, the term has been changed to read "adjust" the values and timings of signals, which, although the equivalent of "adapted," may be more to the Examiner's liking.

Claims 13 and 30 have been amended to clarify the language that is objected to.

In claim 18, the Examiner objects to the reference to "testing a memory" in line 1 and then the method step phrase "at least one memory" in line 5. The Examiner should understand and appreciate that the reference to "at least one memory" on line 5 of claim 18 is not in fact a

reference to the memory of line 1. Instead, this is a reference to "at least one memory **access**" (emphasis added) and is a method step with respect to the plurality of "memory storage locations" noted in the preamble of claim 18. The Examiner should appreciate that former line 5 of claim 18 is a method step of "performing at least one memory access" and is not a reference to a structure. Accordingly, no amendment to claim 18 is believed necessary, and the claim reads accurately as originally worded.

The Examiner states that claims 19-25, 29 and 32-34 are rejected because they depend from claim 8. Actually, these claims depend from claim 18 and it is presumed that the Examiner's reference to claim 8 is a typographical error. Claim 18, as noted above, was properly worded as originally submitted and has been amended to clarify the self-test instruction. As amended, claim 18 is clearly in proper form and claims 19-25, 29 and 32-34 dependent thereon do not contain any additional indefiniteness.

Accordingly, and in view of the above, it is believed that claims 9-11, 13, 14, and 18-34 meet all requirements of 35 USC §112 and therefore clearly and distinctly point out and claim the subject matter of Applicant's invention. Any further rejection thereunder is respectfully traversed.

Claims 1-9, 13, 16-26, 30 and 33 stand rejected under 35 USC §102 as being anticipated by Lo (U.S. Patent 5,661,732). Independent claims 1 and 18 have been amended to point out that the "self-test controller is responsive to a self-test instruction specifying a test methodology to be applied" in order to perform at least one memory access. Support for this amendment is found in Applicants' specification at page 4, lines 4-5 and page 10, line 20 through page 11, line 16 of the originally filed patent specification.

The benefit of the presently claimed invention is that any self-test system which employs a rigid self-test methodology that is tuned to a particular design and fabrication technique by the integrated circuit manufacturer is an inflexible self-test system. Such inflexible systems, while they may perform efficiently in detecting fault in a particular memory implementation, they may not work well in other circumstances without considerable modification. The present invention recognizes that there is a balance between an efficient yet rigid circuit specified test methodology on the one hand and a flexible yet difficult to implement methodology (like the system of Lo) on the other hand.

The Lo patent discloses a programmable micro-processor used to test and characterize on-chip memory arrays. Before the memory test can be accomplished, the micro-code must be loaded by scanning with a desired pattern (see column 1, lines 31-33 of Lo). Lo neither discloses nor suggests that a self-test instruction is used to specify a test methodology to be applied by the self-test controller such that the self-test controller may be configured by the self-test instruction to implement different memory test methodologies.

In Lo, each memory test methodology is specified by a plurality of micro-code instructions, and these are described in detail as "micro-programming examples" in columns 12-16 of the Lo patent. The system of Lo enables different tests to be performed, but requires careful and time-consuming preparation of the micro-code instructions to be loaded in the micro-code array. Moreover, the nature of these micro-code instructions requires a detailed knowledge of the physical configuration of the memory array under test, as well as detailed knowledge of the precise operation and control of the self-test controller itself.

The present invention provides the above-noted benefit in which the self-test instruction is used to specify a test methodology to configure the self-test controller, thereby providing

additional flexibility without introducing a disadvantageous degree of complexity. Because Lo does not disclose the subject matter of Applicants' independent claims, it cannot anticipate those claims under the provisions of 35 USC §102.

Moreover, assuming that one of ordinary skill in the art would even look to the Lo reference for memory test systems, there would be no motivation to modify the Lo system, since one of ordinary skill in the art would believe that Lo already provides a fully flexible test methodology. In accordance with Lo, further tests can be added to the test methodology by preparing further sets of sequences of micro-code program instructions for loading into the micro-code array. Given the nature of micro-code instructions, i.e., each bit field typically controls some specific part of the hardware circuitry, such as next point of calculation logic, the next address calculation logic or the data pattern generation logic (see Figure 1 of Lo), the circuitry of Lo would have to be extensively modified to operate such that a self-test instruction would implement a corresponding memory test methodology.

Furthermore, not only is there no disclosure of such in Lo, the Lo specifications of the detailed micro-codes indicates that Lo would lead one of ordinary skill in the art away from Applicants' claimed combination of elements and method steps. Accordingly, Lo does not suggest or render obvious any modification and indeed would lead one of ordinary skill in the art away from any such modification.

Because all claims depend on either claim 1 or claim 18 and because the Lo reference fails to anticipate claims 1 and 18, it fails to anticipate the claims dependent thereon, and any further rejection of claims 1-9, 13, 16-26, 30 and 33 as being anticipated by Lo is respectfully traversed.

Claims 10, 11, 14, 27, 28 and 31 stand rejected under 35 USC §103 as unpatentable over Lo in view of Gold (U.S. Patent Publication 2003/0167428). Inasmuch as claims 10, 11, 14, 27, 28 and 31 depend either upon claim 1 of claim 18, the above comments distinguishing claims 1 and 18 from the Lo reference are herein incorporated by reference. Inasmuch as Lo fails to anticipate, fails to render obvious and indeed would lead one of ordinary skill in the art away from Applicants' claims 1 and 18, it fails to support any obviousness rejection of dependent claims 10, 11, 14, 27, 28 and 31. Accordingly, any further rejection of these claims as obvious under 35 USC §103 over the Lo/Gold combination is respectfully traversed.

Claims 12, 15, 29 and 32 stand rejected under 35 USC §103 as unpatentable over Lo in view of Correale (U.S. patent 6,001,662). Inasmuch as claims 12, 15, 29 and 32 depend either upon claim 1 of claim 18, the above comments distinguishing claims 1 and 18 from the Lo reference are herein incorporated by reference. Inasmuch as Lo fails to anticipate, fails to render obvious and indeed would lead one of ordinary skill in the art away from Applicants' claims 1 and 18, it fails to support any obviousness rejection of dependent claims 12, 15, 29 and 32. Accordingly, any further rejection of these claims as obvious under 35 USC §103 over the Lo/Correale combination is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that amended claims 1-34 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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